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CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY

FEEDBACK ANALYSIS REPORT OF STAKEHOLDERS (2023-24)

CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY
Chandubhai S Patel Institute of Technology
V. T. Patel Department of Electronics and Communication Engineering

CURRICULUM FEEDBACK ANALYSIS (Students)

Academic Year: 2023-24

Date: 29/06/2024

Sr. No.	Aspect	Excellent (A)	Very Good (B)	Good (C)	Average (D)	Below Average (E)	Average	Response
1	Curriculum Aspects	53	08	03	03	02	3.82	76.40
2	Teaching Learning & Evaluation	49	10	04	03	03	3.76	75.20
3	Research & Extension Activities	41	25	03	01	01	3.86	77.20
4	Infrastructure and Learning Resources	57	08	02	01	01	3.97	79.40
5	Student Support & Progression	53	12	02	01	01	3.92	78.40
6	Governance & Leadership	49	16	02	01	01	3.87	77.40

Scale — Excellent: 5, Very Good: 4, Good: 3, Average: 2, Below Average: 1

Total No. of Responses: 82

Average (A*5 + B*4 + C*3 +D*2 + E*1)/Total no. of responses,

% Response = (Average*100)/5

Other Comments/Suggestions:

1. Overall positive feedback from students.
2. Learning resources and practical aspects of the curriculum appreciated.
3. Enjoyed hands on/workshops sessions.

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CURRICULUM FEEDBACK ANALYSIS (Alumni)

Academic Year: 2023-24

Date: 29/06/2024

Sr. No.	Aspect	Excellent (A)	Very Good (B)	Good (C)	Satisfac-tory (D)	Need Improvement (E)	Average	Response
1	The curriculum was:	0	3	0	0	0	4.00	80.00
2	The relevance of the curriculum of your degree with respect to your current job/position is:	1	1	1	0	0	4.00	80.00
3	When you meet students, who have taken a similar Program at other universities, you feel that your Program is:	1	1	1	0	0	4.00	80.00
4	Have you participated in any of the extracurricular activities of the Department /University?	3	0	0	0	0	5.00	100.00
5.1	Learning value (in terms of skills, concepts, knowledge, analytical abilities, or broadening perspectives)	2	1	0	0	0	4.67	93.33
5.2	Applicability/relevance to real life situations	0	3	0	0	0	4.00	80.00
5.3	Extent and depth of content	0	1	2	0	0	3.33	66.67

5.4	Extent of coverage	1	0	2	0	0	3.67	73.33
5.5	Relevance/learning value of project/ training	1	1	1	0	0	4.00	80.00

Scale — Excellent: 5, Very Good: 4, Good: 3, Satisfactory: 2, Need Improvement: 1

Total No. of Responses: 3

Average = (A*5 + B*4 + C*3 +D*2 + E*1)/Total no. of responses

% Response = (Average*100)/5

Other Comments/Suggestions:

1. None.

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CURRICULUM FEEDBACK ANALYSIS (Academic Peers/Teachers/Industry)

Academic Year: 2023-24

Date: 29/06/2024

Sr. No.	Aspect	Excellent (A)	Very Good (B)	Good (C)	Satisfactory (D)	Needs Improvement (E)	Average	Response
I	Content of syllabus	10	2	0	0	0	4.83	96.67
2	Relevance of syllabus to industry/research requirements	9	3	0	0	0	4.75	95.00
3	Course outcomes are well defined	10	2	0	0	0	4.83	96.67
4	Sufficient reading materials and digital resources provided	9	3	0	0	0	4.75	95.00
5	Incorporation of advanced topics	7	5	0	0	0	4.58	91.67
6	Pedagogy proposed has a desired balance between theory and practical	11	1	0	0	0	4.92	98.33
7	Assessment methods are fair, measuring the outcomes	10	2	0	0	0	4.83	96.67
8	Project component in the course, (if applicable)	6	2	0	0	0	3.17	95.00
9	Industrial training/ practical exposure in the course, (if applicable)	8	0	0	0	0	3.33	100.00

Scale — Excellent: 5, Very Good: 4, Good: 3, Satisfactory: 2, Need Improvement: 1

Total No. of Responses: 12

Average = (A*5 + B*4 + C*3 +D*2 + E*1)/Total no. of responses

% Response = (Average*100)/5

Other Comments/Suggestions:

1. Fundamentals understanding is good

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CURRICULUM FEEDBACK ANALYSIS (Employers)

Academic Year: 2023-24

Date: 29/06/2024

Sr. No.	Aspect	Strongly Agree (A)	Agree (B)	Neutral (C)	Disagree (D)	Strongly Disagree (E)	Average	Response
I	Technical knowledge and skills of the graduate(s) are up to date.	2	4	0	0	0	4.33	86.67
2	Curriculum provides adequate knowledge and training to the students.	2	4	0	0	0	4.33	86.67
3	The graduate(s) exhibits problem solving, leadership & managerial skills.	0	5	1	0	0	3.83	76.67
4	The graduate(s) maintain good interpersonal relations with their colleagues and seniors.	1	4	1	0	0	4.00	80.00
5	The graduate(s) volunteer themselves for new initiatives.	1	3	2	0	0	3.83	76.67
6	The graduate(s) mould themselves as per need of organization.	1	4	0	0	0	3.50	70.00
7	Curriculum facilitated the graduate(s) to attain the desired competency level.	2	3	1	0	0	4.17	83.33
8	Curriculum enriched the moral values among the graduate(s).	3	3	0	0	0	4.50	90.00
9	The Teaching-learning process prepared them for teamwork.	4	2	0	0	0	4.67	93.33

10	Communication skills of students are good.	2	3	0	0	0	3.67	73.33
11	The graduate(s) display sensitivity towards colleagues of varied background and competency levels	1	4	1	0	0	4.00	80.00

Scale — Excellent: 5, Very Good: 4, Good: 3, Satisfactory: 2, Need Improvement: 1

Total No. of Responses: 6

Average = (A*5 + B*4 + C*3 +D*2 + E*1)/Total no. of responses

% Response = (Average*100)/5

Other Comments/Suggestions:

1. Proactive participation of students in technical/Nontechnical events appreciated. Such number of students can be scaled up

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FEEDBACK ACTION TAKEN REPORT OF STAKEHOLDERS (2023-24)

CHARUSAT

Date: 1/6/2024

Subject: Action Plan from various feedback received

Reference Department: EC Department

1. **Action plan from Feedback received from employers.**

#	Suggestion	Action Plan
1	FPGA Based Design should be in the curriculum	Course content is revised for the course EC319: Design, Testing and Verification (Refer Annexure – I, Proceedings 20.01)

2. **Action plan from Feedback received from Teachers (End semester course feedback)**

#	Suggestion	Action Plan
1	Electronics Communication based course should be in the curriculum	New Course Entitled Communication Systems is introduced in Curriculum. (Refer Annexure – II, Proceedings 20.01)

3. **Action plan from Feedback received from Alumni**

#	Suggestion	Action Plan
1	Concept of System on Chip should be in the curriculum.	Concept of System on Chip is introduced the course EC319: Design, Testing and Verification (Refer Annexure – I, Proceedings 20.01)

4. **Action plan from Feedback received from final year students**

#	Suggestion	Action Plan
1	FPGA Based Design should be in the curriculum	Course content is revised for the course EC319: Design, Testing and Verification (Refer Annexure – I, Proceedings 20.01)

5. Action plan from Feedback received from Parents.

#	Suggestion	Action Plan
1	Electronics Communication based course should be in the curriculum	New Course Entitled Communication Systems is introduced in Curriculum. (Refer Annexure – II, Proceedings 20.01)

Dr. Upesh Patel
HoD, EC Department,
FTE, CHARUSAT

CHANDUBHAI S PATEL INSTITUTE OF TECHNOLOGY

FACULTY OF TECHNOLOGY & ENGINEERING

V.T. PATEL DEPARTMENT OF ELECTRONICS AND COMMUNICATION

EC319: DESIGN, TESTING AND VERIFICATION OF DIGITAL CIRCUITS`

Annexture- I

Credit and Hours:

Teaching Scheme	Theory	Practical	Total	Credit
Hours/week	3	2	5	4
Marks	100	50	150	

Pre-requisite Course:

- Digital Electronics

Outline of the Course:

Sr. No.	Title of the Unit	Minimum Number of Hours
1	FPGA based Design	12
2	System on Chip Design	13
3	Introduction to Testing	05
4	Fault Modelling	05
5	Design for testability	05
6	Verification	05
	Total Hours (Theory):	45
	Total Hours (Lab):	30
	Total Hours:	75

Detailed Syllabus:

1	**FPGA based Design**	**12 Hours**	**30%**
1.1	Hierarchical design, controller (FSM), FSM issues, timing issues, pipelining, resource sharing, metastability, synchronization setup/hold time of various types of flip-flops, synchronization between multiple clock domains, reset recovery, proper resets.		
1.2.	Design and analysis of synchronous sequential circuits, Designing with of Melay and Moore based FSM, Optimization of Finite State Machines, Timing issues in sequential machines		
2	**System on Chip Design**	**13 Hours**	**30%**
2.1	Introduction to System Approach,Motivation, design, programming, optimization, and use of modern System-on-a-Chip (SoC) architectures, Components in the system: processor, memory and connectivity. Hardware and Software in the SoC, programmability versus performance. Approaches to designing a SoC		
2.2	Basics SoC Chip:Time, Area, Power, Reliability, and Configurability: Design-space formulation andexploration, Costs and metrics (energy, area, runtime, reliability and predictability), Quantitative design and analysis.		
3	**Introduction to Testing**	**05 Hours**	**10%**
3.1	Testing philosophy, Role of testing, Digital and analog circuit testing, Technology trends affecting testing.		
3.2	Test economics, Defining cost, Benefit-cost analysis, The rule of ten, Yield.		
4	**Fault Modelling**	**05 Hours**	**10%**
4.1	Defects- Errors-Faults, Level of fault models, Single stuck-at fault, Fault Equivalence, Fault Dominance, ATPG		
5	**Design for testability**	**05 Hours**	**10%**
5.1	Functional vs. Structural Testing, scan methods ,controllability and observability, Scan insertion, Scan chain,		
6	**Verification**	**05 Hours**	**10%**
6.1	Importance of verification, Verification plan, Verification flow,		
6.2	Levels of verification, Verification methods and languages, Functional Verification: Introduction to testing bench, Test bench architecture, Types of test benches, Case study		

Self-Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Course Outcome (Cos):

At the end of the course student will be able to:

CO1	Understand and Apply the concepts of state machines to design digital systems and solve real time problems with FPGA
CO2	Discriminate testing and verification concepts for the system
CO3	Identify possible physical defects and model them as logical faults to determine their concerned test vectors.
CO4	Perform functional and timing verification.

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	-	-	-	-	-	-	1	1	2
CO2	2	3	3	-	-	-	-	3	3	3	3	-
CO3	3	3	2	-	-	1	-	2	-	2	-	-
CO4	2	2	3	2	3	-	3	-	3	-	3	3

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) No correlation "-"

Instructional Method and Pedagogy:

1. At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
2. Lectures will be conducted with the aid of multi-media projector, black board, OHP etc. 3. Attendance is compulsory in lectures and laboratory which carries a 5% component of the overall evaluation.
4. Minimum two internal exams will be conducted and average of two will be considered as a part of 15% overall evaluation.
5. Assignments based on course content will be given to the students at the end of each unit/topic and will be evaluated at regular interval. It carries a weightage of 5%.
6. Surprise tests will be conducted which carries 5% component of the overall evaluation. 7. Minimum tutorials which include solution of minimum numerical under each head will be carried

out in laboratory.

Recommended Study Material:

- **Text Books:**

1. Miron Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, John Wiley and Sons/ revised by IEEE
2. Essetinal of electrionic testing,Michal bushnell,Vishwani D Agrawal. Kluwer academic publishers new york, boston, dordrecht, london, moscow

- **Reference Books:**

1. Spear, Chris, Tumbush, Greg, SystemVerilog for Verification A Guide to Learning the Test-bench Language Features, Springer
2. Janick Bergeron, Writing Test benches-Functional Verification of HDL Models, Springer

- **Web Material:**

1. http://www.eng.auburn.edu/~strouce/elec4200.html

- **Software:**

Xillinx Altera, EDA playground

Annexture - II

CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY
FACULTY OF TECHNOLOGY & ENGINEERING
V.T. Patel Department of Electronics and Communication Engineering

Minutes – 20th Meeting of Board of Studies

Date: September 06, 2023, Wednesday
Time: 02:00 pm
Mode: Online

The meeting of the 20th Board of Studies, Department of Electronics and Communication (E&C) Engineering, Faculty of Technology, Charotar University of Science and Technology (CHARUSAT) was held online as per schedule.

The following members were present:

1.	Dr. Upesh Patel	**Chairman**	HoD, Department of E&C Engineering, CSPIT
2.	Dr. Trushit Upadhyaya	**Member**	Professor, Department of E&C Engineering, CSPIT
3.	Dr. Y.P.Kosta	**Member**	Professor, Department of E&C Engineering, CSPIT
4.	Dr. Arpita Patel	**Member**	Associate Professor, Department of E&C Engineering, CSPIT
5.	Dr. Jitendra Chaudhari	**Member**	Associate Professor, Department of E&C Engineering, CSPIT
6.	Dr. Killol Pandya	**Member**	Associate Professor, Department of E&C Engineering, CSPIT
7.	Dr. Poonam Thanki	**Member**	Assistant Professor, Department of E&C Engineering, CSPIT
8.	Dr. Jayesh Pabari	**Member**	Scientist, Physical Research Laboratory (PRL), Ahmedabad
9.	Mr. Bhaskar Trivedi	**Member**	Vice President, Intech Systems, Ahmedabad
10.	Dr. Jignesh Patel	**Member**	Founder, Energy System Engineering, Baroda
11.	Mr. Pinal Patel	**Member**	Distinguished Alumni & Associate Director, e-infochips, An Arrow Company
12.	Sreelakshmi Kurup (20EC037)	**Member**	Student representative, Department of E&C Engineering, CSPIT
13.	Kartik Singh (20EC081)	**Member**	Student representative, Department of E&C Engineering, CSPIT

The following members could not remain present:

1.	Dr. Sanjeev Gupta	**Member**	Dean (Academics) An initiative by Arcelor Mittal University.
2.	Mr. Nilesh Ranpura	**Member**	Director, e-infochips, An Arrow Company, Ahmedabad
3.	Dr. Amit Bhatt	**Member**	Pro Vice-Chancellor, Dayanand Sagar University, Bangalore
4.	Dr. Upena Dalal	**Member**	Professor, Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat
5.	Dr. Brijesh Kundaliya	**Member**	Assistant Professor, Department of E&C Engineering, CSPIT

Agenda Proceedings & Resolutions: -

Item 20.01: For Discussion: To review and approve the Teaching & Examination scheme and detailed syllabus of B.Tech Second year and Third year Electronics and Communication Engineering for the academic year 2024-25.

Proceedings 20.01:

- Board of Studies members reviewed and discussed the teaching scheme and detailed syllabus of B Tech under the Choice Based Credit System (CBCS). The following new courses are introduced or the credit scheme has been changed. The courses are listed below:

Sr. No	Semester	Subject code and name	Remarks
1	3	EC264: Communication Systems	New subject introduced
2	4	EC265: Electromagnetics & Wave Propagation	New subject introduced
3	5	EC319: Design, Tersting and Verification	A few content updated

Resolution 20.01:

- The Board approved the teaching scheme and syllabi of the B. Tech program Second-year and Third year courses with a few suggestions. The teaching and examination scheme along with the detailed syllabus is attached as **Annexure I**.

Item 20.02: For Discussion: To review and approve the Elective Courses from SWAYAM/NPTEL for B.Tech Final year Electronics and Communication Engineering for the academic year 2024-25.

Proceedings 20.02 :

- Board of Studies members reviewed and discussed the detailed syllabus of Elective courses. The courses are listed below:

Sr. No	Semester	Subject code and name	Remarks
1	7	OCEC4001: Digital Image Processing (P.E III)	SWAYAM/NPTEL Course
2	7	OCEC4002: Satellite Communication(P.E III)	SWAYAM/NPTEL Course
3	7	OCEC4003: An Introduction to Coding Theory (P.E III)	SWAYAM/NPTEL Course
4	7	OCEC4004: Advanced 3G and 4G Wireless Mobile Communication (P.E IV)	SWAYAM/NPTEL Course
5	7	OCEC4005: Radar Systems (P.E IV)	SWAYAM/NPTEL Course
6	7	OCEC4006: Fiber Optic Communication Technology (P.E IV)	SWAYAM/NPTEL Course
7	7	OCEC4007: VLSI Design Flow: RTL to GDS (P.E IV)	SWAYAM/NPTEL Course
8	7	OCEC4008: Data Communication & Networking	SWAYAM/NPTEL Course
9	7	OCEC4009: RF & Microwave Engineering	SWAYAM/NPTEL Course

Resolution 20.02:

- The Board approved the syllabus of courses from SWAYAM/NPTEL and a sample syllabus is attached as an **Annexure II**.

Item 20.03: For Discussion: To discuss and approve Ph.D. course work for the admission year 2022-23 batch.

Proceedings 20.03 :

- Ph.D. course work structure was discussed which introduces Department Domain Specific Course I and II, Supervisor Specific Course. along with its detailed structure, methodology, subjects, teaching and examination scheme was presented to the board members.

Resolution 20.03:

- BoS members appreciate Ph.D. course work proposal and approve the teaching and examination scheme. The details along with the list of the courses in the coursework are attached as **Annexure III**.

Item 20.04: For Discussion: Discussion and action taken on the feedback of the stakeholders

Proceedings 20.04 :

- A summary of Curriculum feedback Analysis (feedbacks from students, alumni, academic peers, employers) and action taken report was presented.

Resolution - 20. 04:

- The Board reviewed the suggestion and recommendation implemented in the syllabus based on stakeholders' feedback and analysis of corporate demands and found it appropriate.
- The details and official communication regarding the same are attached as **Annexure IV**.

Item 20.05: For Discussion: Outcome-Based Education (OBE): Attainment & Action Taken

Proceedings 20.05 :

- Board of Studies members reviewed and discussed outcome-based education attainment with the blooms taxonomy level and action taken for. Members appreciate the syllabus design format and the concept of the micro-projects to be implemented in the subjects.

Resolution - 20. 05:

- The Board approved the syllabus of courses aligned with the OBE (Outcome Based Education) and a sample syllabus is attached as **Annexure V.**

Item 20.06: For Discussion: Analysis and discussion on the semester end results of the students and steps taken for the remedial actions.

Proceedings 20.06 :

- The University examination results were discussed with BoS members. Last three academic years' results comparison was carried out. Total number of students having distinction, first class and second class was presented to board members.
- Action plan and on-going activities of department were also discussed for the improvement of the overall result.

Resolution 20.06:

- BoS member found results satisfactory for all the years of B.Tech. The Year-on-year Result Analysis and remedial actions' document are attached as an **Annexure VI**.

Item 20.07: For Discussion: The synopsis approval of research scholars of the department.

Proceedings 20.07 :

- A Synopsis of PhD research scholars were presented to the board members.
- BoS members discussed the articles published by the research scholars in Wos/SJR journals and conferences.

Resolution 20.07:

- Board members appreciated that the department promotes research publications in WoS/SJR-indexed journals.
- Details of research scholars' publications are attached as **Annexure VII.**

Item 20.08: For Discussion: Additional Agenda: Innovation in pedagogy

Proceedings 20.08 :

- BoS Chairman Gave information about the design Thinking. The Workshop arranged for the faculty member. Two days workshop was arranged by HRDC-CHARUSAT for faculty members. The detail of the expert is as under.
- Dr. Bhaumik Nagar - Sr. Faculty in the New Media Design program, and Vice Activity Chairperson Continuing Education Programme, National Institute of Design – Ahmedabad.
- The points Covered are as under.

- An Insight into learning, Emotions: experience and expressions, Basics of design thinking, Creative Thinking and Problem Solving, Prototyping and testing.

Resolution 20.08:

- The faculty members will embed the concepts of the design thinking in their respective courses. BoS members appreciated the concept.

Item 20.09: For Discussion: Additional Agenda: Department clubs and the activities

Proceedings & Resolution 20.09:

- BoS Chairman Gave information about the various technical and nin technical clubs at the department.
- The list of planned activities under each club were discussed. The board members appreciate the initiative and the activies under various clubs by students.

The meeting ended with a vote of thanks.

Dr. Upesh Patel
Chairman, BoS, EC Department,
FTE, CHARUSAT

Date: September 06, 2023