

**CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY**

**V. T. Patel Department of Electronics & Communication Engineering**

**M. Tech. (Communication System Engineering)**

**Semester : II**

**EC708: Digital VLSI Design**

---

**Credit Hours:**

**90**

---

**A Objective of the Course:**

This course will introduce the student to the fundamentals of digital VLSI design, including Microelectronics, MOS technology and transistor. Different Aspects of MOS inverters: static and dynamic characteristics. MOS Logic circuits like combinational, sequential logic and dynamic logic circuits, Designs of semiconductor memories and BiCMOS logic circuits and Ultra-fast VLSI circuits and systems.

**B Out line of the Course:**

Sr. No.	Title of the Unit	Minimum number of hours
1.	A review of microelectronics and introduction to MOS technology and MOS transistors	12
2.	MOS Inverters	14
3.	MOS logic circuits	16
4.	Semiconductor Memories	06
5.	BiCMOS logic circuits	06
6.	Ultra fast VLSI circuits and system- Introduction to GaAs technology	06

Total hours (Theory): 60

Total hours (Lab): 30

Total: 90

---

**C Detailed Syllabus:**

This will provide details about topics under each units of the course.

<b>1. A review of microelectronics and introduction to MOS technology and MOS transistors</b>	hours 06	App. Weightage in %	10%
1.1 VLSI Design Flow, Design hierarchy, Design Methodology, nMOS,pMOS,CMOS fabrication process		6	Hr.
1.2 MOS structures, MOS transistor operation		6	Hrs.

	MOSFET current-voltage characteristic, MOSFET Scaling and Small geometry effects, MOSFET Capacitance			
2.	<b>MOS Inverters</b>	hours	06	App. Weightage in % 10%
2.1	MOS Inverter static characteristics: Resistive load inverter, Inverters with n-type MOSFET load, CMOS Inverter		6	Hrs.
2.2	MOS Inverter switching characteristic and interconnect effects : Calculation of delay time, Inverter design with delay constraints, Estimation of interconnect parasitic, Switching power dissipation of CMOS inverters		8	Hr.
3.	<b>MOS Logic circuits</b>	hours	12	App. Weightage in % 20%
3.1	Combination of MOS logic circuits		6	Hrs.
3.2	Sequential MOS logic circuits		4	Hrs.
3.3	Dynamic logic circuits		6	Hrs.
4.	<b>Semiconductor Memories</b>	hours	12	App. Weightage in % 20%
4.1	DRAM		1	Hrs.
4.2	SRAM		1	Hrs.
4.3	Non volatile Memory		2	Hrs.
4.4	Flash Memory		2	Hrs.
5.	<b>BiCMOS logic circuits</b>	hours	13	App. Weightage in % 21%
5.1	Introduction		1	Hrs.
5.2	BJT structure and operation, Dynamic behavior of BJTs		2	Hrs.
5.3	Basic BiCMOS circuits: Static behavior		1	Hrs.
5.4	Switching delay in BiCMOS logic circuits		2	Hrs.
6.	<b>Ultra fast VLSI circuits and system- Introduction to GaAs technology</b>	hours	13	App. Weightage in % 21%
6.1	Ultra fast system		2	Hrs.
6.2	GaAs structure and technological development		2	Hrs.
6.3	MESFET based design		1	Hrs.

**D Instructional Methods and Pedagogy:**

- Multimedia Projector
- OHP
- Audio Visual Presentations
- Chalk + Board
- White Board
- Online Demo
- Charts

**E Student Learning Outcomes / objectives:**

- Able to Design a digital VLSI system
- Able to take analysis of MOS electrical characteristics
- Able to design different MOS logical circuits
- Able to simulate on VLSI software
- Able to implement on FPGA/CPLD.

**F Recommended Study Material:****Reference books:**

1. CMOS digital integrated circuits: Analysis and Design, Sung-Mo-Kang, Usuf Leblebici, Tata McGrawhill, 2003
2. Basic VLSI Design, Douglas Pucknell, PHI, 1999.
3. Modern VLSI Design. Wayne Wolf, Person Education, 2001
4. Introduction to VLSI circuits and systems, John Uyemura, Wiley, 2002.

**Reading Materials, web materials with full citations:**

1. <http://www.eng.auburn.edu/~strouce/elec4200.html>

**Other materials (e.g. how to write journals, charts, codes, software and hardware etc.)**

1. Lab Manuals
2. FPGA/CPLD Kit
3. Hand Outs
4. Assignments
5. Question Bank

[BACK](#)